

**Appl. No. 10/050,334**

**REMARKS**

Claims 16-26 are pending in the application with claims 16 and 18 amended herein.

The Office requires a title that is clearly indicative of the invention and the Applicants herein amend the title to comply with the requirement.

Claims 16-20 and 22-26 stand rejected under 35 USC 103(a) as being unpatentable over Kitamura in view of Fukuzumi. Applicants request reconsideration.

Applicants note that the Detailed Action does not specifically list claim 21 as being rejected and that the Office Action Summary page lists claim 21 as being objected to. Even so, pages 4-5 of the Office Action describes grounds for rejection of claim 21. Applicants traverse the grounds for rejection of claim 21, however, it appears that such grounds of rejection were intended to be withdrawn in favor of objecting to claim 21 as setting forth allowable subject matter, but depending from a rejected base claim. Accordingly, Applicants request that the Office confirm that the grounds for rejection of claim 21 should be stricken from the record and, in their place, provide a statement of reasons for allowance of claim 21 in the next Office Action.

Amended claim 16 sets forth a capacitor construction that includes, among other features, a surface area enhancement layer over a substrate, a first capacitor electrode over the enhancement layer, a capacitor dielectric layer over the first electrode, and a second capacitor electrode over the dielectric layer. The enhancement layer has an outer surface area per unit area that is greater than an inner surface area per unit area of the enhancement layer. The first electrode has an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit

**Appl. No. 10/050,334**

area of the substrate. The first electrode does not comprise the enhancement layer. The amendment to claim 16 is supported at least by page 15, lines 6-15 of the present specification.

Pages 2-3 of the Office Action allege that Kitamura discloses the subject matter of claim 16. It does not appear that Fukuzumi is relied upon to remedy any deficiencies of Kitamura with regard to claim 16 since no portion of the Office Action provides any statement to such effect. To the extent that the Office relies upon Fukuzumi in rejecting claim 16, Applicants request that the next Office Action clearly explain the pertinence of each reference pursuant to 37 CFR 1.104(c)(2).

The Office Action essentially alleges that the stack electrode having the lamination structure shown in Fig. 2D and discussed in Paragraph [0052] of Kitamura discloses the first capacitor electrode of claim 16. The Kitamura stack electrode includes a doped polysilicon outer layer 2A and a doped inner layer 2C having a hemispherical grain surface 2D. Paragraph [0051] states that doped outer layer 2A may be doped by crystallization from a doped amorphous silicon film or by introducing an impurity by either an impurity diffusion or an ion-implantation. Kitamura does not in any way disclose or suggest that doped outer layer 2A may be undoped. Accordingly, Kitamura clearly contemplates that the stack electrode of Fig. 2D, as well as of Fig. 2E, comprises both doped outer layer 2A and doped inner layer 2C.

Reference to claim 16 reveals that the claimed first capacitor electrode has an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit area of the substrate. Accordingly, the characteristics

*Appl. No. 10/050,334*

of the first capacitor electrode are not expressed in terms of total inner surface area or total outer surface area, but are instead expressed in terms of surface area per unit area. In this manner, the inner and outer surface areas can be compared on a basis independent of a particular electrode shape or configuration. The inherent nature of a unit area, as clearly known to those of ordinary skill, is that the unit area is the same for every surface being compared. That is, the unit area for the inner surface of the first capacitor electrode is identical to the unit area for the outer surface and for the substrate. The first capacitor electrode of claim 16 exhibits the property of having a surface area within a unit area of the electrode inner surface that is greater than the surface area within a unit area of a substrate outer surface. Also, the surface area within a unit area of the electrode outer surface is greater than the surface area within a unit area of the substrate outer surface.

As readily known to those of ordinary skill, it is also inherent in any discussion of surface area per unit area that smooth surfaces exhibit the same surface area per unit area. Surface area per unit area is thus one way to describe roughness or ruggedness of a surface. As is plainly shown in Fig. 2D of Kitamura, all the surfaces of doped outer layer 2A are smooth. Doped outer layer 2A is, in fact, a "stopper layer" against formation of hemispherical grains, as acknowledged on page 3 of the Office Action. Also, the surface of doped inner layer 2C that contacts doped outer layer 2A is also smooth. The only non-smooth surface disclosed by Kitamura is the surface of doped inner layer 2C that has a hemispherical grain surface 2D. By comparison, all of the surfaces of silicon substrate 41 of Kitamura are also smooth. Accordingly, Kitamura does not disclose or suggest any two surfaces of an electrode that both have surface areas per unit area that are greater than

*Appl. No. 10/050,334*

the surface area per unit area of a substrate surface. It is thus impossible for Kitamura to disclose the claim 16 first capacitor electrode with an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit area of the substrate.

Applicants assert that the proper electrode of Kitamura for comparison purposes to claim 16 is the stack electrode that includes both doped outer layer 2A and doped inner layer 2C, as described in Paragraph [0052]. Since both outer layer 2A and inner layer 2C are doped and contact one another, it is clear that both structures will form a part of any resulting electrode. Further, Kitamura expressly states that the lower electrode disclosed therein is a "stack electrode" having a "lamination structure." Kitamura thus clearly contemplates that both layers will form a part of the subject electrode.

In the context of the present specification, and thus the present claims, the terms inner and outer surface of a layer or structure are used with relation to the process for forming the layer or structure. That is, when a layer is formed on a substrate, the inner surface of the layer is the surface formed on the substrate. Correspondingly, the outer surface of the layer is the opposing outward surface. As successive layers are formed over the initial layer, each layer, as well as any subsequent structure formed from the layers, retains the demarcation of inner and outer surfaces.

In comparing Kitamura or Fukuzumi to the present claims, the convention that should be used for denoting inner and outer surfaces is the convention set forth in the present specification and claims, rather than any other convention that may be used in the cited art. Accordingly, for the purpose of comparison to claim 16, the hemispherical grain

3

**Appl. No. 10/050,334**

surface 2D of the stack electrode in Kitamura constitutes the outer surface of the stack electrode. Similarly, the surface of the Kitamura stack electrode that contacts insulator layers 48 and 48b, as well as portions of such surface that do not contact such layers, constitutes the inner surface of the stack electrode. It is thus readily apparent that Kitamura fails to disclose or suggest the first capacitor electrode set forth in claim 16.

In addition, the capacitor construction of claim 16 further includes a surface area enhancement layer over the substrate that has an outer surface area per unit area that is greater than an inner surface area per unit area of the enhancement layer. The first electrode does not comprise the enhancement layer. Review of Kitamura reveals that such reference does not provide any disclosure or suggestion of the claimed enhancement layer as can be readily appreciated from descriptions above regarding the deficiencies of Kitamura.

Claims 17-21 depend from claim 16 and are patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested. For example, amended claim 18 sets forth that the enhancement layer includes rugged polysilicon and claim 19 sets forth that the rugged polysilicon is undoped. Kitamura does not disclose or suggest and is not alleged to disclose or suggest such an enhancement layer. As indicated above, it is not apparent from the Office Action that Fukuzumi is relied upon in any way to reject claim 16, accordingly, claims 16-21 are deemed patentable.

Claim 22 sets forth a capacitor construction that includes, among other features, an opening in an insulative layer over a substrate, a hemispherical grain (HSG) polysilicon layer over sides of the opening but not over a bottom of the opening, a conformal first

*Appl. No. 10/050,334*

capacitor electrode on the polysilicon, a capacitor dielectric layer on the first electrode, and a second capacitor electrode over the dielectric layer. The first electrode is sufficiently thin that it has a rugged outer surface with an outer surface area per unit area greater than an outer surface area per unit area of the substrate underlying the first electrode. Pages 3-4 of the Office Action rely upon Kitamura as allegedly disclosing the subject matter of claim 22 with the exception of an HSG layer over sides of the opening but not over the bottom, and relies upon Fukuzumi as allegedly disclosing such feature.

The bottom of page 3 of the Office Action provides a discussion of Fukuzumi allegedly disclosing the subject matter of claim 21. However, it is apparent that a portion, perhaps a very significant portion, of the paragraph at the bottom of page 3 is missing. The second paragraph of page 4 provides brief additional comments regarding combination of Fukuzumi and Kitamura. Even so, Applicants take the position that the missing text renders the Office Action as not compliant with 37 CFR 1.104(c)(2) requiring a clear explanation the pertinence of each reference. Acting in good faith, Applicants herein distinguish the pending claims from Fukuzumi considered alone or in combination with Kitamura on the basis of teachings readily apparent from the text of such references. If Applicants' remarks herein are not found sufficient to overcome the present rejections, then Applicants assert that a new, non-final action is warranted containing the complete grounds for rejection that appear to be missing from the Office Action.

Applicants note that the last paragraph of page 3 of the Office Action refers to hole portions 5 in polysilicon film 4 over insulating interlayer 2 containing lower electrode 7. The described structures are uniquely shown in Figs. 1-6 of Fukuzumi. Accordingly, Applicants

***Appl. No. 10/050,334***

assume that the Office views the structures shown in such figures as the most pertinent portions of Fukuzumi.

Applicants note that claim 22 includes an insulative layer, a HSG layer, a first electrode, a dielectric layer, and a second electrode. By comparison, the intermediate structure shown in Fig. 4 of Fukuzumi does not form a capacitor since it lacks a dielectric layer on the first electrode and it also lacks a second electrode over the dielectric layer, as set forth in claim 22. The structure of Fig. 4 thus fails to disclose every element of claim 22.

It appears that the Office relies on polysilicon film 4 as allegedly disclosing the HSG polysilicon layer of claim 22. However, as shown in Figs. 5 and 6 of Fukuzumi and described in Paragraph [0079], polysilicon film 4 is removed and is never comprised by a capacitor construction having first and second electrodes and a dielectric layer therebetween.

In addition, it appears that the Office relies upon hole portions 5 as allegedly disclosing the claim 22 opening in an insulative layer over a substrate. However, hole portions 5 are clearly described as being formed in polysilicon film 4. As readily known to those of ordinary skill, polysilicon is a semiconductor and not an insulator. Accordingly, hole portions 5 are not formed in an insulative layer.

At least for the reasons described above, Fukuzumi fails to disclose or suggest every element of claim 22. Applicants acknowledge that Kitamura is relied upon in combination with Fukuzumi. Fukuzumi allegedly remedies the deficiency of Kitamura in failing to disclose the HSG layer over the sides of the insulative layer opening but not over

*Appl. No. 10/050,334*

the bottom. As can be readily appreciated from the discussion above, Fukuzumi fails to remedy the deficiencies of Kitamura at least because polysilicon layer 4 of Fukuzumi is not formed over the sides of an opening in an insulative layer. Further, the claim 22 HSG layer is comprised by a capacitor construction having a dielectric layer and a second electrode. Polysilicon layer 4 of Fukuzumi is never comprised by a capacitor construction having a dielectric layer on a first electrode and a second electrode over the dielectric layer. Fukuzumi thus cannot be considered to disclose or suggest adding polysilicon layer 4 to the Kitamura capacitor. Fukuzumi clearly discloses that polysilicon layer should be removed. At least for such additional reasons, Kitamura in view of Fukuzumi fail to disclose or suggest every element of claim 22.

Claims 23-26 depend from claim 22 and are patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested. Applicants herein establish adequate reasons to distinguish the cited art and to establish the patentability of claims 16-26. Applicants request allowance of all pending claims in the next Office Action.

Further, the Applicants received a copy of a Form PTO-1449 with the present Office Action having the Examiner's initials next to most references, but missing from the A. W. Ott, et al. article listed under Other References. Applicants request consideration of the article and initialing of the PTO-1449.

Applicants note that a Supplemental IDS was filed on May 8, 2002 prior to the mailing date of the present Office Action, but an initialed Form PTO-1449 has not been received indicating consideration of the cited references. To the extent the PTO-1449 has

**Appl. No. 10/050,334**

not already been initialed in the file, such consideration and initialing is requested at this time, and returning of a copy to the undersigned.

Respectfully submitted, 

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**Appl. No. 10/050,334**

Application Serial No. .... 10/050,334  
Filing Date ..... January 15, 2002  
Inventor ..... Vishnu K. Agarwal  
Assignee ..... Micron Technology, Inc.  
Group Art Unit ..... 2813  
Examiner ..... Y. Huynh  
Attorney's Docket No. .... MI22-1913  
Title: Capacitor Constructions With Enhanced Surface Area (as amended)

**VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING  
RESPONSE TO JULY 30, 2002 OFFICE ACTION**

**In the Specification**

The replacement specification paragraphs incorporate the following amendments. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

The Title has been amended as follows:

~~Capacitor Fabrication Methods and~~ Capacitor Constructions With Enhanced Surface Area

The Abstract has been amended as follows:

A capacitor fabrication method may include ~~atomic layer depositing a conductive barrier layer to oxygen diffusion over the first electrode. A method may instead include chemisorbing a layer of a first precursor at least one monolayer thick over the first electrode and chemisorbing a layer of a second precursor at least one monolayer thick on the first precursor layer, a chemisorption product of the first and second precursor layers being comprised by a layer of a conductive barrier material. The barrier layer~~

**Appl. No. 10/050,334**

~~may be sufficiently thick and dense to reduce oxidation of the first electrode by oxygen diffusion from over the barrier layer. An alternative method may include~~ forming a first capacitor electrode over a substrate, the first electrode having an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit area of the substrate. A capacitor dielectric layer and a second capacitor electrode may be formed over the dielectric layer. The method may further include forming rugged polysilicon over the substrate, the first electrode being over the rugged polysilicon. Accordingly, the outer surface area of the first electrode can be at least 30% greater than the outer surface area of the substrate without the first electrode including polysilicon.

### **In the Claims**

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

*Appl. No. 10/050,334*

16. (amended) A capacitor construction comprising:

a surface area enhancement layer over a substrate, the enhancement layer having an outer surface area per unit area that is greater than an inner surface area per unit area of the enhancement layer;

a first capacitor electrode over a substrate the enhancement layer, the first electrode having an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit area of the substrate, and the first electrode not comprising the enhancement layer;

a capacitor dielectric layer over the first electrode; and

a second capacitor electrode over the dielectric layer.

18. (amended) The construction of claim 16 ~~further comprising~~ wherein the enhancement layer comprises rugged polysilicon over the substrate, the first electrode being over the rugged polysilicon.

**-END OF DOCUMENT-**